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466	7590	11/21/2007		
YOUNG & THOMPSON 745 SOUTH 23RD STREET 2ND FLOOR ARLINGTON, VA 22202			EXAMINER KROFCHECK, MICHAEL C	
			ART UNIT 2186	PAPER NUMBER
			MAIL DATE 11/21/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/750,954	Applicant(s) AIGO, TAKAO	
	Examiner Michael Krofcheck	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 September 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the amendment filed on 9/7/2007.
2. Claims 1, 3-4, 6, 8-9, 11-12, 14 have been amended.
3. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not disclose of any "new tasks" as amended into claims 1, 3-4, 6, 8-9, 11, and 14, or inputting new tasks, or a number of new tasks and tasks in execution as first priority. Fig. 3 of the specification, specifically step s15, shows that the number of current tasks is compared with a maximum number of high priority tasks. Nowhere is it indicated that a number of new tasks combined with a number of current tasks is compared with a maximum number of high priority tasks.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neil et al., US patent 6085287, Johnson et al., US patent 63082485, and Hooman et al., US patent application publication 2003/0172104.

9. With respect to claims 1 and 6, O'Neil teaches of a disk array control apparatus/method comprising: a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory (fig. 2; item 26; column 3, lines 55-57); and

wherein said second element adjusts a number of activated ones of the according to the calculated cache hit ratio (fig. 2; item 28; column 4, lines 34-39).

O'Neil fails to specifically teach of a second element constructed and arranged so that when new tasks are input to the disk array control apparatus the second element executes the new tasks as a first priority unless a number of the new tasks and tasks in execution exceeds a first number, and executes the new tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority.

However, Johnson teaches of a second element constructed and arranged so that when tasks are input to the disk array control apparatus the second element executes the tasks as a first priority unless a number of the tasks and tasks in execution exceeds a first number (fig. 8; column 9, lines 20-62; where the number of tasks executed are not to exceed a minimum number), and

executes the tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority (fig. 8; column 9, lines 20-62; where if the minimum is exceeded a task is put to sleep (2nd priority). A sleeping task is of a lower priority than an active task).

The combination of O'Neil and Johnson fails to specifically teach of inputting new tasks and executes the tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority.

However, Hooman teaches of inputting and prioritizing new tasks (abstract, paragraph 19-21).

The combination of O'Neil, Johnson and Hooman teaches of executes the tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority (Johnson, fig. 8; column 9, lines 20-62; in the combination the new tasks are also put in sleep state if the minimum number active tasks is active).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil and Johnson at the time of the invention to include the task management of Johnson in O'Neil. Their motivation would have been to limit spikes in workload, and thus achieve better performance (Johnson, column 2, lines 34-39).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil, Johnson, and Hooman at the time of the invention to include new tasks in the task managing of the combination of O'Neil, Johnson. Their motivation would have been provide a greater impact than that of just managing current tasks.

10. Claims 2 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neil, Johnson and Hooman in further view of Bala US patent 6351844.

11. With respect to claims 2 and 7, the combination of O'Neil, Johnson and Hooman fails to specifically teach of wherein the number of activated ones of the tasks decreases when the calculated cache hit ratio is above a prescribed value and increases when the calculated cache hit ratio is below the prescribed value.

However, Bala teaches of wherein the number of activated ones of the tasks decreases when the calculated cache hit ratio is above a prescribed value and increases when the calculated cache hit ratio is below the prescribed value (column 8,

lines 34-46; if the cache hit rate is high, the threshold is raised so no more traces are examined (lower number of tasks). If it is low, the threshold is lowered so that an increasing number of traces are examined (higher number of tasks). Since the cache hit rate being high or low is used to vary the threshold, there must be a cache hit rate threshold that signifies a high or a low cache hit rate).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil, Johnson, Hooman, and Bala at the time of the invention to implement the cache system identifying hot traces of Bala in the cache memory system of the combination of O'Neil, Johnson and Hooman. Their motivation would have been to efficiently identify the hot traces to capture the current working set in the cache memory (Bala, column 8, lines 38-40).

12. Claims 2-4, 7-9, 11, 13, 14, 16 rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neil, Niitaka, Williams and Ryan US patent 5367656.

13. With respect to claims 2 and 7, the combination of O'Neil, Johnson and Hooman fails to specifically teach of wherein the number of activated ones of the tasks decreases when the calculated cache hit ratio is above a prescribed value and increases when the calculated cache hit ratio is below the prescribed value.

However, Ryan teaches of wherein the number of activated ones of the tasks decreases when the calculated cache hit ratio is above a prescribed value and increases when the calculated cache hit ratio is below the prescribed value (fig. 1, 5; column 8, lines 63-column 9, line 7).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil, Johnson, Hooman, and Ryan at the time of the invention to include the cache predictive prefetching system of Ryan in the cache memory system of the combination of O'Neil, Johnson and Hooman. Their motivation would have been to lower the cache miss ratio (Ryan, column 2, lines 40-42).

14. With respect to claims 3 and 8, Ryan teaches of a first element constructed and arranged so that the first element calculates a cache hit ratio at a cache memory (fig. 1, 5; column 2, lines 58-63);

wherein said second element executes only the first priority tasks when the cache hit ratio is above a prescribed value and executes both the first priority tasks and second priority tasks when the cache hit ratio is below the prescribed value (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs and regular cache accessing occurs. The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are high priority tasks since they are required for processor to carry out the program. The miss prediction is a low priority task because it just enhances the performance of the cache memory, it is not required for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out).

O'Neil teaches of a disk array control apparatus/method comprising: a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

Johnson teaches of a second element constructed and arranged so that when tasks are input to the disk array control apparatus the second element executes the tasks as a first priority unless a number of the tasks and tasks in execution exceeds a first number (fig. 8; column 9, lines 20-62; where the number of tasks executed are not to exceed a minimum number), and

executes the tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority (fig. 8; column 9, lines 20-62; where if the minimum is exceeded a task is put to sleep (2nd priority). A sleeping task is of a lower priority than an active task).

Hooman teaches of inputting and prioritizing new tasks (abstract, paragraph 19-21).

The combination of Ryan, O'Neil, Johnson and Hooman teaches of executes the tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority (Johnson, fig. 8; column 9, lines 20-62; in the combination the new tasks are also put in sleep state if the minimum number active tasks is active).

15. With respect to claim 4, Ryan teaches of a cache hit determination unit constructed and arranged to determine whether or not the I/O process request is causing a cache hit at a cache memory (fig. 2; column 4, lines 7-14);

a cache hit ratio monitor unit constructed and arranged to calculate and output a cache hit ratio within some period of time by using a determination result of the cache hit determination unit (fig. 1, 5; column 2, lines 58-63; as it must be known if the request is a cache hit or miss to calculate the ratio, the hit ratio must be calculated based on whether the requests were hits or misses in the cache memory); and

an execution task selection unit constructed and arranged to assign each said I/O process request to either the first or second priority tasks (fig. 1, 3-5; column 4, lines 7-14; upon the operand/data request, the request are sent to determine if they result in a cache hit or miss (first priority I/O)),

the execution task selection unit assigning said I/O process request to the first priority tasks when the cache hit ratio is not less than some prescribed value and assigning said I/O process request to the second priority tasks when the cache hit ratio is less than the prescribed value (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs (second priority) and regular cache accessing occurs (first priority). The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are first priority tasks since they are required for processor to carry out the program. The miss prediction is a second priority task because it just enhances the performance of the cache memory, it

is not required for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out (first priority I/O execution unit)).

O'Neil teaches of a disk array control apparatus comprising: a host I/O reception unit arranged so that the host I/O reception unit receives as an input an I/O process request from a host computer, the I/O reception unit generating as an output the I/O process request (fig. 2; item 22, column 3, lines 54-65) and a disk cache memory (fig. 2; item 18).

Johnson teaches of an I/O process execution unit that executes tasks input to the disk array control apparatus as a first priority unless a number of the tasks and tasks in execution as the first priority exceeds a first number (fig. 8; column 9, lines 20-62; where the number of tasks executed are not to exceed a minimum number), and

executes the tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority (fig. 8; column 9, lines 20-62; where if the minimum is exceeded a task is put to sleep (2nd priority). A sleeping task is of a lower priority than an active task).

Hooman teaches of inputting and prioritizing new tasks (abstract, paragraph 19-21).

The combination of Ryan, O'Neil, Johnson and Hooman teaches of executes the tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the

second priority (Johnson, fig. 8; column 9, lines 20-62; in the combination the new tasks are also put in sleep state if the minimum number active tasks is active).

16. With respect to claim 9, Ryan teaches of a control method comprising the steps of: inputting an I/O process request from a host computer (fig. 2; column 4, lines 7-10);

determining whether the I/O process request is causing a cache hit at a cache memory (fig. 2; column 4, lines 7-14);

calculating a cache hit ratio within some period of time based on results of the determining step (fig. 1, 5; column 2, lines 58-63; as it must be known if the request is a cache hit or miss to calculate the ratio of such, the hit ratio must be calculated based on whether the requests were hits or misses in the cache memory);

assigning the I/O process request to the first priority tasks when the cache hit ratio is not less than some prescribed value; and assigning the I/O process request to the second tasks and low priority tasks when the cache hit ratio is less than the prescribed value (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs and regular cache accessing occurs. The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are first priority tasks since they are required for processor to carry out the program. The miss prediction is a second priority task because it just enhances the performance of the cache memory, it is not required for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out).

O'Neil teaches of a disk array control method comprising: calculating a cache hit ratio within some period of time at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

Johnson teaches of executing the tasks as a first priority unless a number of the tasks and tasks in execution as the first priority exceeds a first number (fig. 8; column 9, lines 20-62; where the number of tasks executed are not to exceed a minimum number), and

executing the tasks as a second priority when the number of the tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority (fig. 8; column 9, lines 20-62; where if the minimum is exceeded a task is put to sleep (2nd priority). A sleeping task is of a lower priority than an active task).

Hooman teaches of inputting and prioritizing new tasks (abstract, paragraph 19-21).

The combination of Ryan, O'Neil, Johnson and Hooman teaches of executing the tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority (Johnson, fig. 8; column 9, lines 20-62; in the combination the new tasks are also put in sleep state if the minimum number active tasks is active).

17. With respect to claims 11 and 14, the combination of Ryan, O'Neil, Niitaka, and Williams teach of the limitations of the claims as previously described.

18. With respect to claims 13 and 16, O'Neil teaches of a disk cache memory which is accessed by one of the first or second priority tasks; and a plurality of disks which are accessed by said one of the first or second priority tasks when said disk cache memory does not have data for said one of the first or second priority tasks (fig. 2; column 3, lines 39-53; as taught in the combination, the different commands are of the different priorities).

19. Claims 5, 10, 12, 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan, O'Neil, Johnson and Hooman as applied to claims 4, 9, 11, 14 respectively, and further in view of Horii et al., JP 08-077025 A.

20. With respect to claims 5, 10, 12, 15 the combination of Ryan, O'Neil, Johnson and Hooman fails to specifically teach of a task priority change unit constructed and arranged to dynamically change the second priority task to one of the first priority tasks after starting execution of the second priority task, the task priority change unit changing the one of the first priority tasks whose priority has been changed to the first priority back to the second priority tasks at execution termination time.

However, Horii teaches of a task priority change unit constructed and arranged to dynamically change the second priority task to one of the first priority tasks after starting execution of the second priority task, the task priority change unit changing the one of the first priority tasks whose priority has been changed to the first priority back to the second priority tasks at execution termination time (paragraph 0009).

It would have been obvious to one of ordinary skill in the art having the teachings of Ryan, O'Neil, Johnson, Hooman, and Horii at the time of the invention to modify the

priority of the tasks while they are being executed as taught in Horii. Their motivation would have been to avoid the inversion phenomenon of priority, where a low priority task is executed before a high priority task (Horii, paragraph 0005).

Response to Arguments

21. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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